WHAT IS CLAIMED IS:

1. A method of transferring data comprising:

receiving a transfer request;

determining if the transfer request is a write to a memory location;

if the transfer request is a write to a memory location, then sending the transfer request as a posted request; else

determining a number of available transfer request entries in a posted-write first-in-first-out memory; and

if the number of transfer request entries available is greater than a first number; then

sending the transfer request as a posted request; else

waiting to send the transfer request as a posted request.

2. The method of claim 1 wherein the transfer request is made by a video capture card.

3. The method of claim 1 wherein the transfer request is made by a graphics processor.

4. The method of claim 1 wherein the transfer request is sent over a HyperTransport bus.

5. The method of claim 1 wherein the number of pending posted requests is determined by an arbiter.

6. The method of claim 1 wherein the first number is programmable.

7. The method of claim 1 wherein the first number has a value of one.

8. A method of transferring data comprising:

maintaining a first number of tokens;

receiving a plurality of posted requests;

if a remaining number of the first number of tokens is less than a first number, forwarding one of the plurality of posted requests as a non-posted request; else

not forwarding the one of the plurality of posted requests as a non-posted request.

9. The method of claim 8 wherein the first number of tokens is one.

10. The method of claim 8 wherein the first number of tokens is maintained by an address decoder.

11. The method of claim 8 further comprising:

receiving a response from a pending non-posted request; and

incrementing the number of available tokens by one.

12. The method of claim 11 further comprising when the number of tokens is incremented above the first number, then forwarding the one of the plurality of posted requests as a non-posted request.

13. An integrated circuit comprising:

an arbiter configured to track a number of available entries in a posted request FIFO;

a plurality of clients coupled to the arbiter; and

a HyperTransport bus coupled to the arbiter;

wherein the arbiter receives peer-to-peer requests from the plurality of clients and provides posted requests to the posted request FIFO, and

when the number of available entries in the posted request FIFO is equal to a first number, then preventing the plurality of clients from sending peer-to-peer requests.

14. The integrated circuit of claim 13 wherein the plurality of clients includes a graphics processor.

15. The integrated circuit of claim 14 wherein the plurality of clients further includes a PCI-to-PCI bridge.

16. The integrated circuit of claim 13 wherein the number of pending peer-to-peer requests is incremented by one for each granted posted request.

17. The integrated circuit of claim 16 wherein the number of pending peer-to-peer requests is decremented by one for each peer-to-peer request provided by a receive FIFO.

18. The integrated circuit of claim 13 further comprising when the number of pending peer-to-peer requests is less than the first number, allowing the number of clients to issue a peer-to-peer request.

19. The integrated circuit of claim 18 wherein the first number is one.